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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,147	07/16/2003	Robert Ian Gresham	18065	1214

26794 7590 09/12/2008

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EXAMINER	
CAVALLARI, DANIEL J	
ART UNIT	PAPER NUMBER
2836	
MAIL DATE	DELIVERY MODE
09/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,147	GRESHAM, ROBERT IAN	
	Examiner	Art Unit	
	DANIEL CAVALLARI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *1-5,7,8,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see Remarks, page 6, filed 5/28/2008, with respect to the rejection(s) of claim(s) 1-5, 7-9, 12 and 13 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as disclosed below.

Claims 6 and 11 are cancelled. Claim 10 stands withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 3-5, 7, 8, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Filoramo et al. (US 6,433,647).

In regard to claim 1

A switch circuit comprising:

a first circuit portion (side A, figure 2) corresponding to a first input port (VLO,I);

a second circuit portion (side B) corresponding to a second input port (VLO,Q); and

an output port (VIF/IF-Output, see figures 1 and 2), wherein each of the first and second circuit portions include at least one first transistor (Q3a/Q3b, figure 2) providing a portion of an

isolation channel, at least one second transistor (Q5a/Q5b) providing a portion of a transmit channel, and at least two third transistors (Q1a/Q1b) for providing a control bias for selecting either the transmit channel or the isolation channel; and wherein each third transistor (Q1a/Q1b) of the first circuit portion is coupled at its base directly to a base of a corresponding third transistor of the second circuit portion (see figure 2), and to a control voltage source (VRF).

In regard to claim 3

The switch circuit of claim 1, wherein the at least two third transistors of each of the first and second circuit portions provides a control bias for selecting which of the first and second input ports are coupled to the output port (see figure 2).

In regard to claim 4

The switch circuit of claim 1, wherein the at least one first transistor comprises two transistors (Q3a, Q4a, figure 2) and the at least one second transistor comprises two transistors (Q5a, Q6a).

In regard to claim 5

The switch circuit of claim 1, wherein the at least one second transistor comprises three transistors (Q4a, Q5a, Q6a, see figure 2).

In regard to claim 7

The switch circuit of claim 1, wherein respective emitters of the at least one first transistor (Q3a, figure 2) and the at least one second transistor (Q5a) are coupled to each other (via Q1a and

Q2a).

In regard to claim 8

The switch circuit of claim 7, wherein the respective emitters of the at least one first transistor (Q3a, figure 2) and the at least one second transistor (Q5a) are additionally coupled to a collector of a respective third transistor (Q2a via Q1a, see figure 2).

In regard to claim 13

The switch circuit of claim 1, wherein the at least one second transistor comprises three transistors (Q4a, Q5a, Q6a, see figure 2), and the respective emitters of the at least one first transistor and three second transistors are coupled to each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Filoramo et al. (US 6,433,647) in view of Limberg (US 3,798,376).

In regard to Claim 2

Incorporating all arguments above of the switching device taught by Filoramo et al. (hereinafter referred to as Filoramo), Filoramo further teaches the use of semiconductor devices but fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Filoramo into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight, increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

In regard to claim 12

Filoramo teaches the at least two third transistors of each of the first and second circuit portions (Q1a, Q2a of the first circuit portion and Q1b and Q2b of the second circuit portion, see figure 2) provides a control bias for selecting which of the first and second input ports (VLO, I and VLO, Q, see figure 2) are coupled to the output port, and the at least one first transistor comprises two transistors (Q3a, Q4a) and the at least one second transistor comprises two transistors (Q5a, Q6a).

Filoramo further teaches the use of semiconductor devices but fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Filoramo into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight, increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

Allowable Subject Matter

Claim 9 is allowed.

The following is an examiner's statement of reasons for allowance:

The closest prior art of Aoki (JP 2001-274707A) teaches an RF switch circuit that uses a single differential amplifier (10b, see figure 1) used to switch a single input (17) between a first channel and a second channel (PORT2 and PORT3). Prior art of record does not teach providing a first channel for each of the at least two inputs including at least one differential amplifier pair wherein the first channel provides isolation between the two inputs. Providing a second channel for each of the two inputs including a second differential pair wherein the second channel provides coupling between the two inputs. And providing a control bias that selects one of the two inputs and a respective first or second channel.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

/Daniel Cavallari/

August 25, 2008